# UNITED STATES PATENT AND TRADEMARK OFFICE

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/028,320 | 12/28/2001 | Masahiro Taniguchi | 032404-020 | 4754 |

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Platon N. Mandros
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. BOX 1404
Alexandria, VA  22313-1404

| EXAMINER |
|---|
| TORRES, JUAN A |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2631 | |

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| | Application No. | Applicant(s) |
|---|---|---|
| **Office Action Summary** | 10/028,320 | TANIGUCHI, MASAHIRO |
| | Examiner | Art Unit | |
| | Juan A. Torres | 2631 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 May 2005*.

2a)☐ This action is **FINAL**.      2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☒ All   b)☐ Some * c)☐ None of:

   1.☒ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

# DETAILED ACTION

## *Drawings*

The drawings were received on 05/19/2005. These drawings are accepted by

the Examiner.

## *Specification*

The modifications to the specification were received on 05/19/2005. These

modifications are accepted by the Examiner.

## *Claim Objections*

In view of the amendment filed on 05/19/2005, the Examiner withdraws claim

objections of claims 3, 6 and 7 of the previous Office Action.

## *Claim Rejections - 35 USC § 112*

In view of the amendment filed on 05/19/2005, the Examiner withdraws the 35

USC § 112 rejection to claims 5-11 of the previous Office Action.

## *Allowable Subject Matter*

The indicated allowability of claims 1-4 is withdrawn in view of the newly

discovered reference(s) to Schwartz (US 6859563). Rejections based on the newly

cited reference(s) follow.

## *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by
another filed in the United States before the invention by the applicant for patent or (2) a patent
granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Schwartz (US 6859563).

As per claim 1 Schwartz discloses a processing method of JPEG 2000 bit modeling with a significance propagation decoding pass, wherein a processing circuit of bit modeling is simultaneously applied to four bits in one group and processes the four bits in parallel (figure 3 column 12 lines 29-50), the processing circuit simultaneously generating a context and a decision of data changing according to a state of significance flags of a bit to be processed and ambient bit group and a context and a decision of sign bits changing according to a state of the sign bits of the bit to be processed and the ambient bit group; adopting the context and decision of the sign bits only when a value of the bit to be processed is 1 and updating the significance flag; disposing of the context and the decision when the value of the bit to be processed is 0; and updating a processed flag whether the value of the bit to be processed is 1 or 0 (figures 5-8 column 13 line 32 to column 17 line 61 and figure 15 column 23 lines 12-53).

As per claim 2 Schwartz discloses a register which stores a value of data of a bit to be processed (figures 5 and 6 column 13 lines 33-65); a register which stores significance flags and sign bits of the bit to be processed and ambient bit group (figure 13 table 7 column 21 line 56 to column 22 line 40); and a register which stores an unprocessed flag of the bit to be processed (figures 5 and 6 column 13 lines 33-65).

As per claim 3 Schwartz discloses a processing method of JPEG 2000 bit modeling with a magnitude refinement pass, wherein a processing circuit of the bit modeling is simultaneously applied to four bits in one group and processes the four bits in parallel (figure 3 column 12 lines 29-50), the processing circuit referring to significance second bit which is information about as to whether or not a bit to be processed is processed with the magnitude refinement pass at first time, a processed flag and an significance flag so as to make a judgment as to whether or not the bit to be processed is processed; and in the case where the bit to be processed is processed with the magnitude refinement pass, generating a context and a decision of the bit so as to update the processed flag (figure 7 column 16 line 6 to column 18 line 36).

As per claim 4 Schwartz discloses a register which stores a value of data of a bit to be processed (figures 5 and 6 column 13 lines 33-65); a register which stores significance flags of the bit to be processed and ambient bit group (figure 13 table 7 column 21 line 56 to column 22 line 40); and a register which stores a significance second bit which is information about as to whether or not the bit to be processed is processed with the magnitude refinement pass at the first time (column 16 line 6 to column 17 line 30).

As per claim 5 Schwartz discloses a processing method of JPEG 2000 bit modeling with a cleanup pass, wherein a first processing circuit of the bit modeling for, when all bits in a group to be processed are unprocessed, makes a judgment as to whether or not the bits can be processed collectively and when all the bits in the group are insignificant (figure 11 column 19 line 34 to column 20 line 19), generating a special

context and a decision (Figure 15 column 23 line 12-53); and a second circuit of the bit

modeling for not processing processed bits and processing insignificant bits are   .

provided (figure 12 column 20 line 20-63), and the first processing circuit is applied to

one bit  (figure 3 column 12 lines 29-50) and the second processing circuit is applied to

four bits in the group simultaneously so as to process the bits in parallel (figure 3

column 12 lines 29-50).

As per claim 6 Schwartz discloses a processing method of JPEG 2000 bit

modeling with a step of processing significance propagation decoding pass, wherein a

first processing circuit of bit modeling is simultaneously applied to four bits in one group

and processes the four bits in parallel (figure 3 column 12 lines 29-50), the processing

circuit simultaneously generating a context and a decision of data changing according to

a state of significance flags of a bit to be processed and ambient bit group and a context

and a decision of sign bits changing according to a state of the sign bits of the bit to be

processed and the ambient bit group; adopting the context and decision of the sign bits

only when a value of the bit to be processed is 1 and updating the significance flag;

disposing of the context and the decision when the value of the bit to be processed is 0;

and updating a processed flag whether the value of the bit to be processed is 1 or 0

(figures 5-8 column 13 line 32 to column 17 line 61 and figure 15 column 23 lines 12-

53); a step of processing magnitude refinement pass, wherein a second processing

circuit of the bit modeling is simultaneously applied to four bits in one group and

processes the four bits in parallel (figure 3 column 12 lines 29-50), the processing circuit

referring to significance second bit which is information about as to whether or not a bit

to be processed is processed with the magnitude refinement pass at first time, a processed flag and an significance flag so as to make a judgment as to whether or not the bit to be processed is processed; and in the case where the bit to be processed is processed with the magnitude refinement pass, generating a context and a decision of the bit so as to update the processed flag (figure 7 column 16 line 6 to column 18 line 36);a step of processing a cleanup pass, wherein a third processing circuit of the bit modeling for, when all bits in a group to be processed are unprocessed, makes a judgment as to whether or not the bits can be processed collectively and when all the bits in the group are insignificant (figure 11 column 19 line 34 to column 20 line 19), generating a special context and a decision (Figure 15 column 23 line 12-53); and do not process processed bits (figure 12 column 20 line 20-63), and one bit  (figure 3 column 12 lines 29-50) and one bit when processing all the bits collectively and four bits when processing the bits in the same group are processed simultaneously and in parallel (figure 3 column 12 lines 29-50) wherein, when the bit plane is same, then the significance propagation decoding pass, the magnitude refinement pass, and the cleanup pass are processed successively (column 20 lines 20-37).

As per claim 7 Schwartz discloses a processing method of JPEG 2000 bit . modeling with a step of processing significance propagation decoding pass, wherein a first processing circuit of bit modeling is simultaneously applied to four bits in one group and processes the four bits in parallel (figure 3 column 12 lines 29-50), the processing circuit simultaneously generating a context and a decision of data changing according to a state of significance flags of a bit to be processed and ambient bit group and a context

and a decision of sign bits changing according to a state of the sign bits of the bit to be

processed and the ambient bit group; adopting the context and decision of the sign bits

only when a value of the bit to be processed is 1 and updating the significance flag;

disposing of the context and the decision when the value of the bit to be processed is 0;

and updating a processed flag whether the value of the bit to be processed is 1 or 0

(figures 5-8 column 13 line 32 to column 17 line 61 and figure 15 column 23 lines 12-

53); a step of processing magnitude refinement pass, wherein a second processing

circuit of the bit modeling is simultaneously applied to four bits in one group and

processes the four bits in parallel (figure 3 column 12 lines 29-50), the processing circuit

referring to significance second bit which is information about as to whether or not a bit

to be processed is processed with the magnitude refinement pass at first time, a

processed flag and an significance flag so as to make a judgment as to whether or not

the bit to be processed is processed; and in the case where the bit to be processed is

processed with the magnitude refinement pass, generating a context and a decision of

the bit so as to update the processed flag (figure 7 column 16 line 6 to column 18 line

36);a step of processing a cleanup pass, wherein a third processing circuit of the bit

modeling for, when all bits in a group to be processed are unprocessed, makes a

judgment as to whether or not the bits can be processed collectively and when all the

bits in the group are insignificant (figure 11 column 19 line 34 to column 20 line 19),

generating a special context and a decision (Figure 15 column 23 line 12-53); and do

not process processed bits (figure 12 column 20 line 20-63), and one bit  (figure 3

column 12 lines 29-50) and one bit when processing all the bits collectively and four bits

when processing the bits in the same group are processed simultaneously and in parallel (figure 3 column 12 lines 29-50) wherein, when the bit plane is same, three adjacent groups in the bit plane are processed in parallel for each of the significance propagation decoding pass, the magnitude refinement pass, and the cleanup pass (column 27 lines 25-56).

As per claim 8 Schwartz discloses processing a plurality of bits in the bit plane in parallel (figure 3 column 12 lines 29-50).

As per claim 9 Schwartz discloses processing a plurality of bit planes in parallel (column 27 line 64 to column 28 line 31).

As per claim 10 Schwartz discloses a register which stores data bits, sign bits, processed flags, significance flags and significance second bits for a code block size (figures 5 and 6 column 13 lines 33-65 and figure 13 table 7 column 21 line 56 to column 22 line 40).

As per claim 11 Schwartz discloses a register which stores a data bit, a sign bit, a processed flag, a significance flag and a significance second bit for a bit to be processed (figures 5 and 6 column 13 lines 33-65 and figure 13 table 7 column 21 line 56 to column 22 line 40).
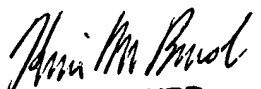
## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 703-

872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).


Juan Alberto Torres
5-31-2005

KEVIN BURD
PRIMARY EXAMINER